



# UNITED STATES PATENT AND TRADEMARK OFFICE

*un*

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,328	02/11/2004	Kiyoshi Kato	0756-7254	8545
31780	7590	01/25/2007		
ERIC ROBINSON PMB 955 21010 SOUTHBANK ST. POTOMAC FALLS, VA 20165			EXAMINER FULK, STEVEN J	
			ART UNIT	PAPER NUMBER
			2891	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/25/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

## Office Action Summary

Application No.

10/775,328

Applicant(s)

KATO ET AL.

Examiner

Steven J. Fulk

Art Unit

2891

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 26 October 2006.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 26, 2006 has been entered.

### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-19, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ovshinsky et al. '471 in view of Mueller '625. The process limitations of detaching and stacking the semiconductor elements found in product claims 5-8 invoke the product-by-process doctrine. Product-by-process claims are not limited to the manipulations of the recited steps, only the structure implied by the steps (*MPEP* § 2113). For example, anticipation of claim 5 does not require that the semiconductor elements be stacked by transferring an element formed over a different substrate.

a. Regarding claims 1, 3, 5, 7, 9, 16-19, 21 and 22, Ovshinsky et al. discloses a semiconductor device (figs. 6A & 6B; col. 18, line 58 – col. 19, line 66) comprising stacked thin film semiconductor circuits each having a thin film transistor (fig. 6A, 232, 234; col. 2, line 39 – col. 3, line 21, DIFET thin film transistors), with an adhesive film (leveling film, 220) and an insulating film (236) formed between semiconductor circuits. The reference discloses a light emitting element (layer 158 of device 232) and a light receiving element (layer 42 of device 234) electrically connected to one of the stacked semiconductor elements; a first electric signal from the respective thin film transistor inputted into the light emitting element and converted into an optical signal; and the optical signal converted into a second electric signal in the light receiving element and inputted into the respective thin film transistor (col. 6, lines 5-23); the light emitting element to comprise a first electrode (154), a second electrode (164) and an electro-luminescent layer (158) laminated between the electrodes; wherein the first electrode, the electro-luminescent layer, and the second electrode are overlapped each other (stack of 154, 158 and 164 is overlapping); and wherein the one of the stacked semiconductor elements has a first crystallized layer (layer 158 of device 232; col. 2, lines 51-53, crystalline thin film devices) and wherein the another one of the stacked semiconductor elements has a second crystallized semiconductor layer (layer 42 of device 234).

Ovshinsky et al. does not explicitly teach the leveling film that holds together the stacked semiconductor circuits to comprise a resin. Mueller teaches a stacked optoelectronic coupling element wherein a resin (fast-curing adhesive) is used to hold together a light emitting device and a light receiving device (fig. 2, col. 2, line 64 – col. 3, line 2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the resin of Mueller as the adhesive leveling film in the device of Ovshinsky et al. One would have been motivated to do this because resin was a well known adhesive used in optoelectronic devices that would have improved the device quality by providing a firm joint between elements and reduced process time by quickly curing (Mueller, col. 2, line 64 – col. 3, line 2).

b. Regarding claims 2, 4, 6, 8, 10 and 16-19, Ovshinsky et al. in view of Mueller discloses all of the elements of the claims as discussed above including an insulating film between the semiconductor elements, but does not explicitly teach the insulating film to be a metal oxide. Mueller teaches a stacked optoelectronic coupling element wherein a metal oxide is formed between the stacked elements (fig. 2, 3; col. 3, lines 15-17).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the metal oxide of Mueller as the insulating film in the optoelectronic device of Ovshinsky et al. One would have been motivated to do this because metal oxides were well known insulating materials used in optoelectronic devices due to their excellent

insulation properties and their transparency (Mueller, col. 3, lines 15-17), which would allow the device to perform its intended function by propagating the optical signal within the device.

c. Regarding claims 11-15, Ovshinsky et al. in view of Mueller discloses all of the elements of the claims as discussed above including using the semiconductor device in a computer or central processing unit (Ovshinsky et al., col. 4, lines 32-38), but does not explicitly teach using the device in a mobile phone, electronic book, electronic card or watch card.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an optoelectronic coupling semiconductor device in a mobile phone, electronic book, electronic card, or watch card. One would have been motivated to do this because all of the devices listed are well known examples of devices that require a central processing unit and relay switches to operate, and using an optoelectronic switching device instead of an electrical relay would have increased the device performance by providing a smaller size, longer life, higher switching rate and faster response time (Mueller, col. 1, lines 21-25).

4. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ovshinsky et al. '471 in view of Mueller '625, and further in view of Yuan et al. '206.

Ovshinsky et al. in view of Mueller teaches all of the elements of the claim as set forth in paragraph 3 above, but the references do not teach the light emitting element to be an organic light emitting device. Yuan et al. teaches a

semiconductor optocoupler device having stacked elements comprising a light emitting device (fig. 1, 104) and light receiving device (102), wherein the light emitting device is an organic light emitting device (¶32).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the organic light emitting device of Yuan et al. in the semiconductor device as taught by Ovshinsky et al. in view of Mueller. One would have been motivated to do this because Yuan et al. taught that organic light emitting devices were capable of being fabricated on any smooth surface at low processing temperatures (¶105), which resulted in less defects formed in the devices and improved their performance (¶102).

#### ***Response to Arguments***

5. Applicant's arguments with respect to the rejection of claims 1-19 and 21 under 35 U.S.C 103(a) have been considered but are moot in view of the new ground(s) of rejection. The rejection set forth in paragraph 3a above describes how Ovshinsky in fact does teach a stack of a first electrode, an electro-luminescent layer, and a second electrode, wherein the layers overlap each other.

6. Applicant's arguments with respect to Ovshinsky's lack of teaching a thin film transistor have been fully considered but they are not persuasive. Ovshinsky describes the DIFET devices as thin film transistors (col. 18, line 58 – col. 19, line 66), and the active layers of the these transistors are clearly thin film semiconductor layers (fig. 6A, device 234: gate 154', gate insulator 156', thin film active layer 42, source/drain layer 164'/166'; device 232: gate 154, gate insulator 156, thin film active layer 158, source/drain layer 164).

**Conclusion**

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven J. Fulk whose telephone number is (571) 272-8323. The examiner can normally be reached on Monday through Friday, 9:30am to 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Steven J. Fulk  
Patent Examiner  
Art Unit 2891  
January 15, 2007



**B. WILLIAM BAUMEISTER**  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800